Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A data latch circuit which samples a digital signal comprising:

a capacitor means having first and second electrodes;

an inverter whose input terminal is connected to the first electrode; and

a switch connected between the input terminal and an output terminal of the inverter,

wherein the switch is turned ON **[[to input]]** and a first potential is input to the second electrode of the capacitor means during a reset period, and

wherein the digital signal is input to the second electrode of the capacitor means during a sampling period after the reset period.

2. (Previously Presented) A data latch circuit which samples a digital signal comprising:

a capacitor means having first and second electrodes;

an inverter whose input terminal is connected to the first electrode;

a first switch connected between the input terminal and an output terminal of the inverter; and

second and third switches connected to the second electrode,

wherein the first switch and the second switch are turned ON to input a first potential to the second electrode of the capacitor means during a reset period, and

wherein the third switch is turned ON to input the digital signal to the second electrode of the capacitor means during a sampling period after the reset period.

3. (Previously Presented) A data latch circuit which samples a digital signal comprising:

a capacitor means having first and second electrodes;

a first inverter whose input terminal is connected to the first electrode;

a switch connected between the input terminal and an output terminal of the first inverter;

a second inverter whose input terminal is connected to the output terminal of the first inverter; and

a clocked inverter whose output terminal and input terminal are connected to the input terminal and an output terminal of the second inverter respectively,

wherein the switch is turned ON to input a first potential to the second electrode of the capacitor means during a reset period, and

wherein the digital signal is input to the second electrode of the capacitor means during a sampling period after the reset period.

4. (Previously Presented) A data latch circuit which samples a digital signal comprising:

a capacitor means having first and second electrodes;

a first inverter whose input terminal is connected to the first electrode;

a first switch connected between the input terminal and an output terminal of the first inverter;

second and third switches connected to the second electrode;

a second inverter whose input terminal is connected to the output terminal of the first inverter; and

a clocked inverter whose output terminal and input terminal are connected to the input terminal and an output terminal of the second inverter respectively,

wherein the first switch and the second switch are turned ON to input a first potential to the second electrode of the capacitor means during a reset period, and

wherein the third switch is turned ON to input the digital signal to the second electrode of the capacitor means during a sampling period after the reset period.

5. (Previously Presented) A data latch circuit which samples a digital signal comprising:

a capacitor means having first and second electrodes;

a first inverter whose input terminal is connected to the first electrode;

a switch connected between the input terminal and an output terminal of the first inverter;

a second inverter whose input terminal is connected to the output terminal of the first

inverter; and

a clocked inverter whose output terminal and input terminal are connected to the input terminal and the output terminal of the first inverter respectively,

wherein the switch is turned ON to input a first potential to the second electrode of the capacitor means during a reset period, and

wherein the digital signal is input to the second electrode of the capacitor means during a sampling period after the reset period.

6. (Previously Presented) A data latch circuit which samples a digital signal comprising:

a capacitor means having first and second electrodes;

a first inverter whose input terminal is connected to the first electrode;

a first switch connected between the input terminal and an output terminal of the first inverter;

second and third switches connected to the second electrode;

a second inverter whose input terminal is connected to the output terminal of the first inverter; and

a clocked inverter whose output terminal and input terminal are connected to the input terminal and the output terminal of the first inverter respectively,

wherein the first switch and the second switch are turned ON to input a first potential to the second electrode of the capacitor means during a reset period, and

wherein the third switch is turned ON to input the digital signal to the second electrode of the capacitor means during a sampling period after the reset period.

7. (Currently Amended) A data latch circuit which samples a digital signal comprising:

a first capacitor means having first and second electrodes;

a second capacitor means <u>having</u> third and fourth electrodes;

an inverter whose input terminal is connected to the first electrode and the third electrode; and

a switch connected between the input terminal and an output terminal of the inverter,

wherein the switch is turned ON **[[to input]]** <u>and</u> a first potential <u>is input</u> to the second

electrode of the first capacitor means and **[[to input]]** a second potential is input to the fourth electrode of the **[[third]]** second capacitor means during a reset period, and

wherein the digital signal is input to the second electrode of the first capacitor means and to the fourth electrode of the second capacitor means during a sampling period after the reset period.

8. (Currently Amended) A data latch circuit which samples a digital signal comprising:

a first capacitor means having first and second electrodes;

a second capacitor means having third and fourth electrodes;

an inverter whose input terminal is connected to the first electrode and the third electrode;

a first switch connected between the input terminal and an output terminal of the inverter;

second and third switches connected to the second electrode; and

fourth and fifth switches connected to the fourth electrode,

wherein the first switch and the second switch are turned ON to input a first potential to the second electrode of the first capacitor means while the fourth switch is turned ON to input a second potential to the fourth electrode of the **[[third]]** second capacitor means during a reset period, and

wherein the third switch is turned ON to input the digital signal to the second electrode of the first capacitor means while the fifth switch is turned ON to input the digital signal to the fourth electrode of the second capacitor means during a sampling period after the reset period.

9. (Previously Presented) A data latch circuit which samples a digital signal comprising:

a first capacitor means having first and second electrodes;

a second capacitor means having third and fourth electrodes;

a first inverter whose input terminal is connected to the first electrode and whose output terminal is connected to the third electrode;

a first switch connected between the input terminal and the output terminal of the first inverter;

a third capacitor means having fifth and sixth electrodes;

a fourth capacitor means having seventh and eighth electrodes;

a second inverter whose input terminal is connected to the fifth electrode and whose output terminal is connected to the seventh electrode;

a second switch connected between the input terminal and the output terminal of the second inverter;

a third inverter whose input terminal is connected to the fourth and eighth electrodes; and

a third switch connected between the input terminal and an output terminal of the third inverter,

wherein the first and second switches are turned ON to input a first potential to the second electrode of the first capacitor means and to input a second potential to the fourth electrode of the third capacitor means during a reset period, and

wherein the digital signal is input to the second electrode of the first capacitor means and to the fourth electrode of the second capacitor means during a sampling period after the reset period.

10. (Previously Presented) A data latch circuit which samples a digital signal comprising:

a first capacitor means having first and second electrodes;

a second capacitor means having third and fourth electrodes;

a first inverter whose input terminal is connected to the first electrode and whose output terminal is connected to the third electrode;

a first switch connected between the input terminal and the output terminal of the first inverter;

a third capacitor means having fifth and sixth electrodes;

a fourth capacitor means having seventh and eighth electrodes;

a second inverter whose input terminal is connected to the fifth electrode and whose output terminal is connected to the seventh electrode;

a second switch connected between the input terminal and the output terminal of the second inverter;

a third inverter whose input terminal is connected to the fourth and the eighth electrodes;

a third switch connected between the input terminal and the output terminal of the third inverter; and

a fifth capacitor connected to the first electrode and the fifth electrode,

wherein the first and second switches are turned ON to input a first potential to the second electrode of the first capacitor means and to input a second potential to the fourth electrode of the third capacitor means during a reset period, and

wherein the digital signal is input to the second electrode of the first capacitor means and to the fourth electrode of the second capacitor means during a sampling period after the reset period.

11. (Previously Presented) The data latch circuit according to, claim 7, wherein the first potential is a potential of 1 or 0 as the digital signal.

12. (Previously Presented) The data latch circuit according to claim 8, wherein the first potential is a potential of 1 or 0 as the digital signal.

13. (Previously Presented) The data latch circuit according to claim 9, wherein the first potential is a potential of 1 or 0 as the digital signal.

14. (Previously Presented) The data latch circuit according to claim 1, wherein the reset period is determined with a sampling pulse from a shift register of the preceding stage while the sampling period is determined with a sampling pulse from a shift register of the present stage.

15. (Previously Presented) The data latch circuit according to claim 2, wherein the reset period is determined with a sampling pulse from a shift register of the preceding stage while the sampling period is determined with a sampling pulse from a shift register of the present stage.

16. (Previously Presented) The data latch circuit according to claim 3, wherein the reset period is determined with a sampling pulse from a shift register of the preceding stage while the sampling period is determined with a sampling pulse from a shift register of the present stage.

17. (Previously Presented) The data latch circuit according to claim 4, wherein the reset

period is determined with a sampling pulse from a shift register of the preceding stage while the sampling period is determined with a sampling pulse from a shift register of the present stage.

18. (Previously Presented) The data latch circuit according to claim 5, wherein the reset period is determined with a sampling pulse from a shift register of the preceding stage while the sampling period is determined with a sampling pulse from a shift register of the present stage.

19. (Previously Presented) The data latch circuit according to claim 6, wherein the reset period is determined with a sampling pulse from a shift register of the preceding stage while the sampling period is determined with a sampling pulse from a shift register of the present stage.

20. (Previously Presented) The data latch circuit according to claim 7, wherein the reset period is determined with a sampling pulse from a shift register of the preceding stage while the sampling period is determined with a sampling pulse from a shift register of the present stage.

21. (Previously Presented) The data latch circuit according to claim 8, wherein the reset period is determined with a sampling pulse from a shift register of the preceding stage while the sampling period is determined with a sampling pulse from a shift register of the present stage.

22. (Previously Presented) The data latch circuit according to claim 9, wherein the reset period is determined with a sampling pulse from a shift register of the preceding stage while the sampling period is determined with a sampling pulse from a shift register of the present stage.

23. (Previously Presented) The data latch circuit according to claim 10, wherein the reset period is determined with a sampling pulse from a shift register of the preceding stage while the sampling period is determined with a sampling pulse from a shift register of the present stage.

24. (Previously Presented) The data latch circuit according to claim 1, wherein the amplitude of the digital signal is comparatively smaller than the width of a power supply voltage which is used for the data latch circuit.

25. (Previously Presented) The data latch circuit according to claim 2, wherein the amplitude of the digital signal is comparatively smaller than the width of a power supply voltage which is used for the data latch circuit.

26. (Previously Presented) The data latch circuit according to claim 3, wherein the amplitude of the digital signal is comparatively smaller than the width of a power supply voltage which is used for the data latch circuit.

27. (Previously Presented) The data latch circuit according to claim 4, wherein the amplitude of the digital signal is comparatively smaller than the width of a power supply voltage which is used for the data latch circuit.

28. (Previously Presented) The data latch circuit according to claim 5, wherein the amplitude of the digital signal is comparatively smaller than the width of a power supply voltage which is used for the data latch circuit.

29. (Previously Presented) The data latch circuit according to claim 6, wherein the amplitude of the digital signal is comparatively smaller than the width of a power supply voltage which is used for the data latch circuit.

30. (Previously Presented) The data latch circuit according to claim 7, wherein the amplitude of the digital signal is comparatively smaller than the width of a power supply voltage which is used for the data latch circuit.

31. (Previously Presented) The data latch circuit according to claim 8, wherein the amplitude of the digital signal is comparatively smaller than the width of a power supply voltage which is used for the data latch circuit.

32. (Previously Presented) The data latch circuit according to claim 9, wherein the

amplitude of the digital signal is comparatively smaller than the width of a power supply voltage which is used for the data latch circuit.

33. (Previously Presented) The data latch circuit according to claim 10, wherein the amplitude of the digital signal is comparatively smaller than the width of a power supply voltage which is used for the data latch circuit.

34. (Previously Presented) The data latch circuit according to claim 4, wherein an output pulse of the shift register of the preceding stage is used for a control terminal of the clocked inverter.

35. (Previously Presented) The data latch circuit according to claim 5, wherein an output pulse of the shift register of the preceding stage is used for a control terminal of the clocked inverter.

36. (Previously Presented) The data latch circuit according to claim 6, wherein an output pulse of the shift register of the preceding stage is used for a control terminal of the clocked inverter.

37. (Previously Presented) The data latch circuit according to claim 1, wherein the data latch circuit is formed by using thin film transistors.

38. (Previously Presented) The data latch circuit according to claim 2, wherein the data latch circuit is formed by using thin film transistors.

39. (Previously Presented) The data latch circuit according to claim 3, wherein the data latch circuit is formed by using thin film transistors.

40. (Previously Presented) The data latch circuit according to claim 4, wherein the data latch circuit is formed by using thin film transistors.

41. (Previously Presented) The data latch circuit according to claim 5, wherein the data latch circuit is formed by using thin film transistors.

42. (Previously Presented) The data latch circuit according to claim 6, wherein the data latch circuit is formed by using thin film transistors.

43. (Previously Presented) The data latch circuit according to claim 7, wherein the data latch circuit is formed by using thin film transistors.

44. (Previously Presented) The data latch circuit according to claim 8, wherein the data latch circuit is formed by using thin film transistors.

45. (Previously Presented) The data latch circuit according to claim 9, wherein the data latch circuit is formed by using thin film transistors.

46. (Previously Presented) The data latch circuit according to claim 10, wherein the data latch circuit is formed by using thin film transistors.

47. (Previously Presented) An electronic device having the data latch circuit according to claim 1, wherein the electronic device is selected from the group consisting of a display, a mobile computer, a game machine, a mobile phone, a navigation system, and a camera.

48. (Previously Presented) An electronic device having the data latch circuit according to claim 2, wherein the electronic device is selected from the group consisting of a display, a mobile computer, a game machine, a mobile phone, a navigation system, and a camera.

49. (Previously Presented) An electronic device having the data latch circuit according to claim 3, wherein the electronic device is selected from the group consisting of a display, a mobile computer, a game machine, a mobile phone, a navigation system, and a camera.

50. (Previously Presented) An electronic device having the data latch circuit according to claim 4, wherein the electronic device is selected from the group consisting of a display, a mobile computer, a game machine, a mobile phone, a navigation system, and a camera.

51. (Previously Presented) An electronic device having the data latch circuit according to claim 5, wherein the electronic device is selected from the group consisting of a display, a mobile computer, a game machine, a mobile phone, a navigation system, and a camera.

52. (Previously Presented) An electronic device having the data latch circuit according to claim 6, wherein the electronic device is selected from the group consisting of a display, a mobile computer, a game machine, a mobile phone, a navigation system, and a camera.

53. (Previously Presented) An electronic device having the data latch circuit according to claim 7, wherein the electronic device is selected from the group consisting of a display, a mobile computer, a game machine, a mobile phone, a navigation system, and a camera.

54. (Previously Presented) An electronic device having the data latch circuit according to claim 8, wherein the electronic device is selected from the group consisting of a display, a mobile computer, a game machine, a mobile phone, a navigation system, and a camera.

55. (Previously Presented) An electronic device having the data latch circuit according to claim 9, wherein the electronic device is selected from the group consisting of a display, a mobile computer, a game machine, a mobile phone, a navigation system, and a camera.

56. (Previously Presented) An electronic device having the data latch circuit according to claim 10, wherein the electronic device is selected from the group consisting of a display, a mobile computer, a game machine, a mobile phone, a navigation system, and a camera.